AMENDMENTS TO THE CLAIMS:

This listing of claims replaces all prior versions and listings of claims in the application:

LISTING OF CLAIMS:

1. (Previously Presented) A processor, comprising:

a crypto unit comprising:

a cipher core configured to cipher data received;

authentication cores configured to authenticate the ciphered data, at least two authentication cores each implementing a different authentication algorithm; and

an authentication buffer configured to store the ciphered data and provide the ciphered data to the authentication cores each in an amount based on the corresponding authentication algorithm implemented.

2. (Previously Presented) The processor according to claim 1, wherein the crypto unit further comprises a plurality of processing contexts.

3. (Currently Amended) The processor according to claim 1, wherein the authentication buffer comprises buffer elements corresponding to a plurality of processing contexts.

4. (Previously Presented) The processor according to claim 3, wherein each of the buffer elements stores data for a respective one of the processing contexts.

5. (Previously Presented) The processor according to claim 4, wherein the buffer elements have a size that is at least as large as a largest authentication algorithm block size implemented by the authentication cores.

6. (Currently Amended) The processor according to claim 1, wherein the crypto unit further comprises a plurality of cipher cores configured to cipher data and the authentication buffer comprises a plurality of authentication buffer elements.

7. (Previously Presented) The processor according to claim 6, wherein the plurality of cipher cores are coupled to the authentication buffer elements via a first multiplexer device and the authentication buffer elements are coupled to the authentication cores via a second multiplexer device.

8. (Previously Presented) The processor according to claim 6, wherein one of the authentication cores processes data in 16-byte blocks and another one of the authentication cores processes data in 64-byte blocks.

9. (Previously Presented) The processor according to claim 8, wherein one of the cipher cores processes data in 8-byte blocks and another one of the cipher cores processes data in 16-byte blocks.

10. (Previously Presented) A method of cryptographic data processing, comprising:

storing ciphered data in blocks having a predetermined size;

storing the data blocks in an authentication buffer; and

providing the ciphered data to authentication cores each in an amount based on a corresponding authentication algorithm implemented by an associated authentication core, at least two authentication cores each implementing a different authentication algorithm.

11. (Previously Presented) The method according to claim 10, further comprising ciphering data received in a first one of a plurality of cipher cores to form the ciphered data.

12. (Previously Presented) The method according to claim 10, further comprising ciphering data received using a first one of a plurality of cipher algorithms to form the ciphered data.

13. (Previously Presented) The method according to claim 10, further comprising authenticating the ciphered data.

14. (Previously Presented) The method according to claim 10, further comprising authenticating the ciphered data using the authentication algorithms.

15. (Previously Presented) The method according to claim 10, further comprising storing the ciphered data in a first one of a plurality of buffer elements in the authentication buffer based upon an associated one of a plurality of processing contexts.

16. (Previously Presented) The method according to claim 10, further comprising ciphering data in a plurality of cipher cores, storing ciphered data in a first one of a plurality of buffer elements in the authentication buffer based upon an associated one of a plurality of processing contexts, authenticating ciphered data in a plurality of authentication cores, and processing a plurality of packets in parallel.

17. (Previously Presented) The method according to claim 10, further comprising determining whether data is to be ciphered.

18. (Previously Presented) A processor, comprising:

a plurality of cipher cores;

an authentication buffer to stored ciphered data from the plurality of cipher cores, the authentication buffer comprising buffer elements corresponding to processing contexts, wherein the authentication buffer is coupled to the plurality of cipher cores via a first bus; and

a plurality of authentication cores to authenticate ciphered data from the authentication buffer, at least two authentication cores each implementing a different authentication algorithm,

wherein the authentication buffer is coupled to the plurality of authentication cores via a second bus and configured to provide the ciphered data to the authentication cores each in an amount based on the corresponding authentication algorithm implemented.

19. (Previously Presented) The processor according to claim 18, wherein a size of at least one of the buffer elements in the authentication buffer is at least as large as a largest authentication algorithm block size implemented by the authentication cores.

20. (Previously Presented) A network switching device, comprising.

a processor comprising a crypto unit comprising:

a cipher core configured to cipher data received;

authentication cores configured to authenticate the ciphered data, at least two authentication cores each implementing a different authentication algorithm; and

an authentication buffer configured to store the ciphered data and provide the ciphered data to the authentication cores each in an amount based on the corresponding authentication algorithm implemented.

21. (Original) The device according to claim 20, wherein the crypto unit includes a plurality of processing contexts.

22. (Original) The device according to claim 21, wherein the authentication buffer includes a number of buffer elements corresponding to a number of processing contexts.

23. (Currently Amended) The device according to claim 22 ~~20~~, wherein each of the buffer elements stores data for a respective one of the processing contexts.

24. (Original) The device according to claim 20, wherein the device includes one or more of a router, network switch, security gateway, storage area network client, and server.

25. (Previously Presented) A network, comprising.

a network switching device comprising a processor comprising a crypto unit comprising:

a cipher core configured to cipher data received;

authentication cores configured to authenticate the ciphered data, at least two authentication cores each implementing a different authentication algorithm; and

an authentication buffer configured to store the ciphered data and provide the ciphered data to the authentication cores each in an amount based on the corresponding authentication algorithm implemented.

26. (Original) The network according to claim 25, wherein the crypto unit includes a plurality of processing contexts.

27. (Original) The network according to claim 26, wherein the authentication buffer includes a number of buffer elements corresponding to a number of processing contexts.

28. (Currently Amended) The network according to claim 27 ~~25~~, wherein each of the buffer elements stores data for a respective one of the processing contexts.

29. (Original) The network according to claim 25, wherein the device includes one or more of a router, network switch, security gateway, storage area network client, and server.

30. (Previously Presented) The processor of claim 1 wherein the authentication buffer is configured to receive unciphered data.

31. (Previously Presented) The processor of claim 30 wherein the authentication buffer is configured to provide the unciphered data to one of the authentication cores in an amount based on an authentication algorithm implemented.

32. (Previously Presented) An integrated circuit chip, comprising:

a processor comprising:

cipher cores configured to cipher data received;

authentication cores configured to authenticate the ciphered data, at least two authentication cores each implementing a different authentication algorithm; and

an authentication buffer configured to store the ciphered data and provide the ciphered data to the authentication cores each in an amount based on the corresponding authentication algorithm implemented.

33. (Previously Presented) The integrated circuit chip of claim 32 wherein the processor further comprises processing contexts.

34. (Previously Presented) The processor of claim 33 wherein the authentication buffer comprises buffer elements corresponding to the processing contexts.